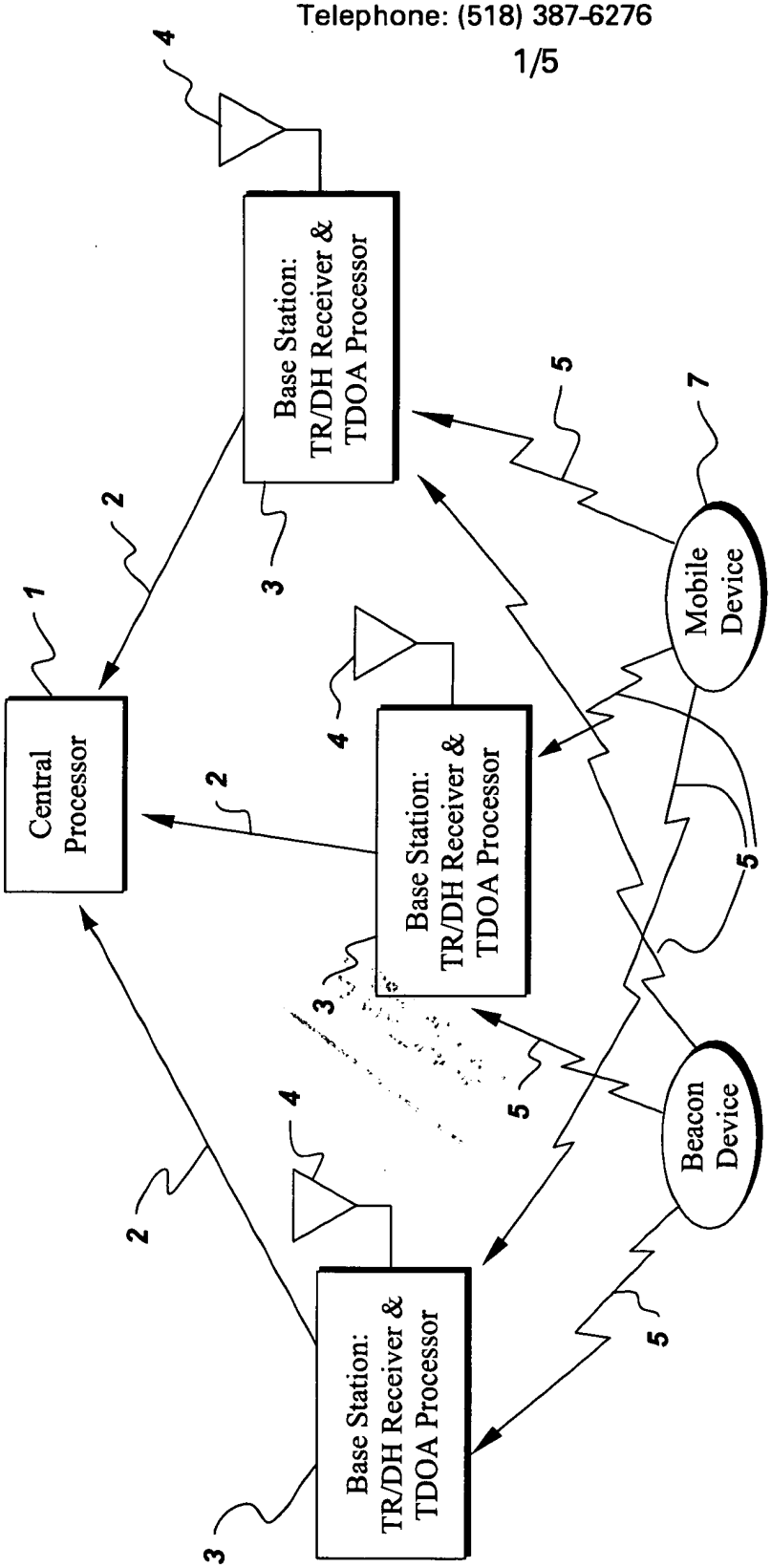

Central Processor
Base Station: TR/DH Receiver & TDOA Processor
Base Station: TR/DH Receiver & TDOA Processor
Base Station: TR/DH Receiver & TDOA Processor
Mobile Device
Beacon Device
1
2
3
4
5
7

Fig. 1

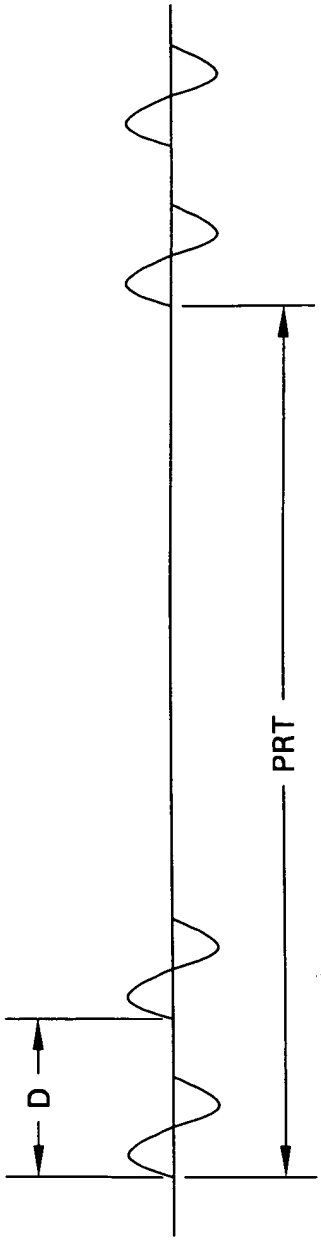

PRT
D

Fig. 2

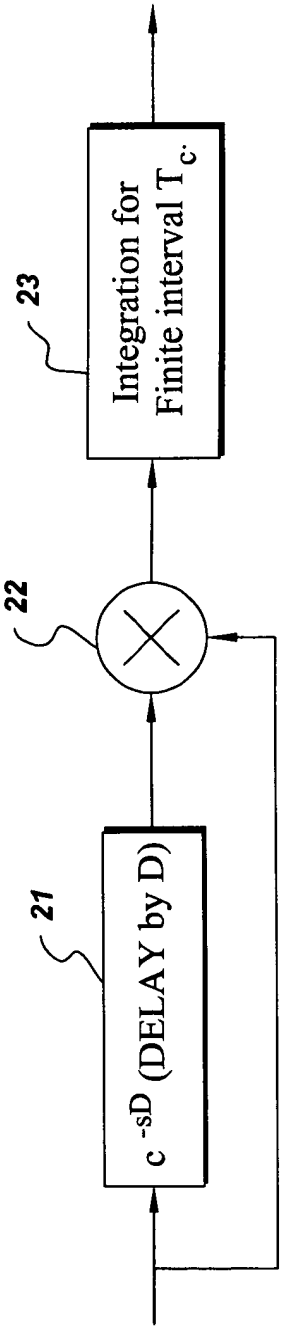

23
Integration for Finite interval T_c
22
21
c^{-sD} (DELAY by D)

Fig. 3

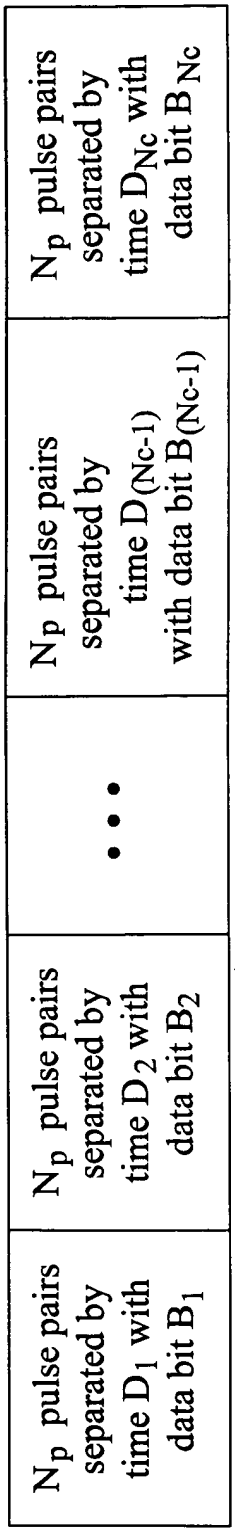

N_p pulse pairs separated by time D_1 with data bit B_1
N_p pulse pairs separated by time D_2 with data bit B_2
• • •
N_p pulse pairs separated by time $D_{(Nc-1)}$ with data bit $B_{(Nc-1)}$
N_p pulse pairs separated by time D_{Nc} with data bit B_{Nc}

Fig. 4

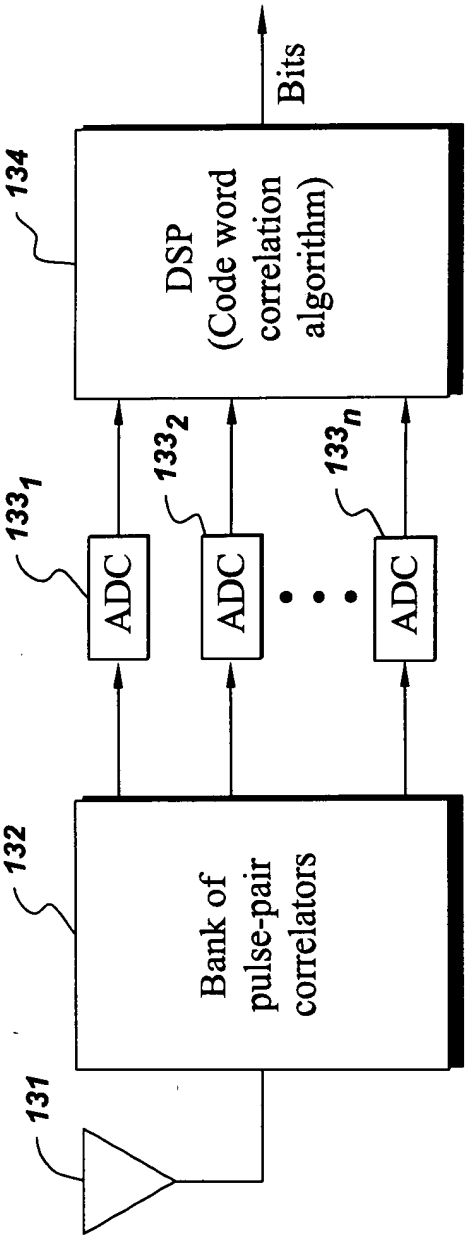

131
132
Bank of pulse-pair correlators
133_1
133_2
133_n
ADC
ADC
ADC
134
DSP (Code word correlation algorithm)
Bits

Fig. 5

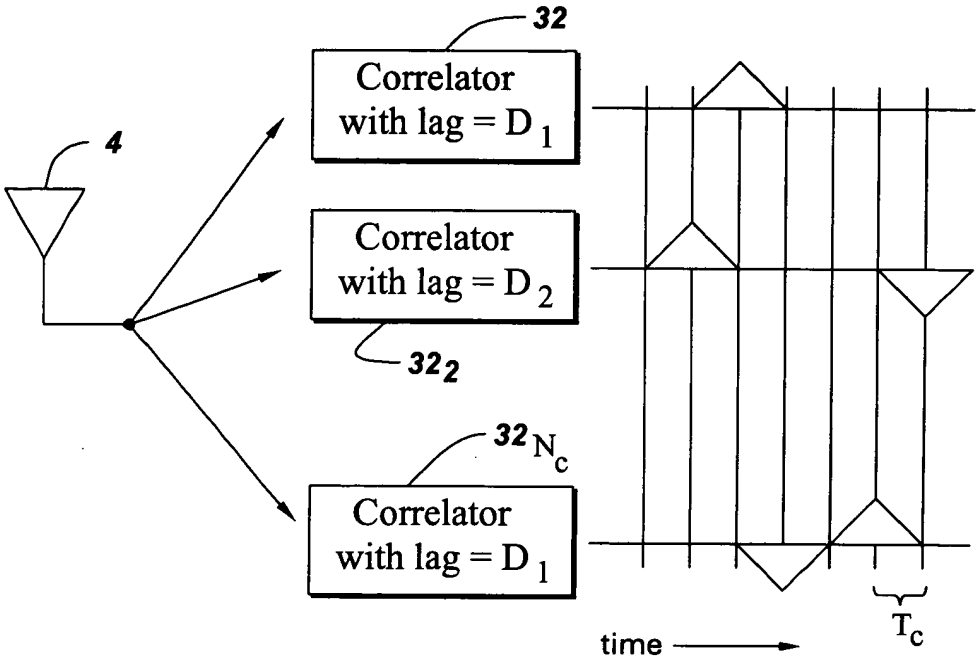

32
Correlator with lag = D_1
4
Correlator with lag = D_2
32_2
32_{N_c}
Correlator with lag = D_1
time
T_c

Fig. 6

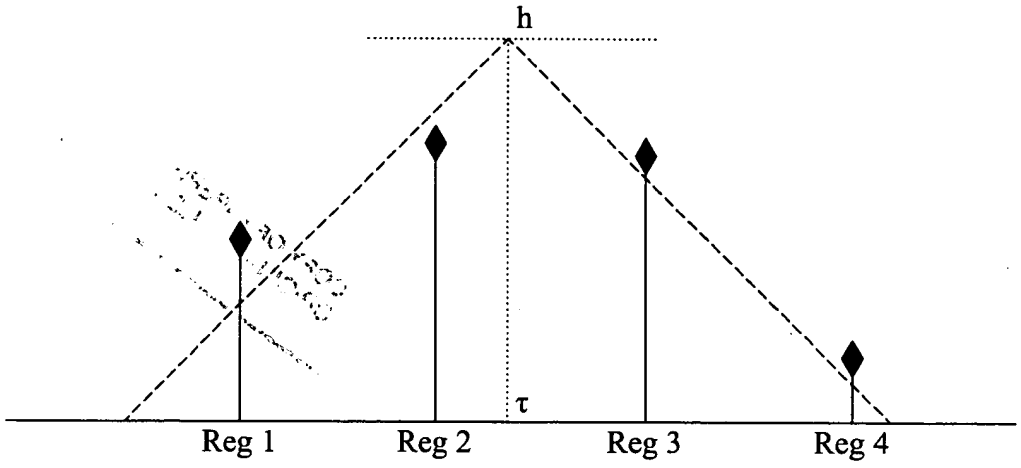
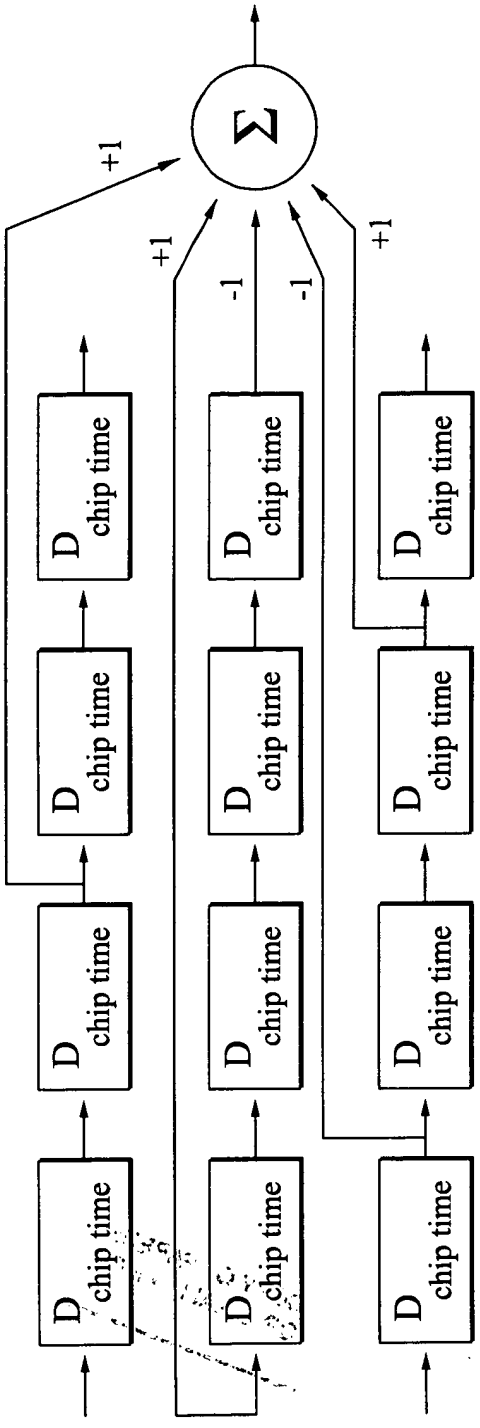

h
τ
Reg 1
Reg 2
Reg 3
Reg 4

Fig. 7



Outputs of pulse-pair
correlators for a range of lags

Fig. 8